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EXAMINER	
YIGDALL, MICHAEL J	

ART UNIT	PAPER NUMBER
2192	

DATE MAILED: 03/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,813	SPRUNT ET AL.	
	Examiner	Art Unit	
	Michael J. Yigdall	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,7-9,18,20,21 and 27-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,7-9,18,20,21 and 27-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is responsive to Applicant's submission filed on December 20, 2005. Claims 1, 3, 4, 7-9, 18, 20, 21 and 27-45 are pending.

Response to Arguments

2. Applicant's arguments have been fully considered but they are not persuasive.

Applicant contends that (a) Larsen does not disclose or suggest a first multiplexer and a second multiplexer in the arrangement that is now recited in claim 1 (remarks, page 11, first paragraph), similarly that (b) there is no disclosure or suggestion in Dreyer of a first multiplexer and a second multiplexer in the recited arrangement (remarks, page 11, last paragraph), and similarly again that (c) Diepstraten does not disclose or suggest the recited arrangement (remarks, page 13, first paragraph).

However, the combination of Larsen, Diepstraten and Dreyer as a whole would have suggested to one of ordinary skill in the art a first multiplexer and a second multiplexer in the arrangement now recited in the claims, as set forth below. Applicant's amendment necessitated the new ground(s) of rejection.

Response to Amendment

3. The rejection of claims 1, 3, 4, 7-9, 18, 20, 21 and 27-45 under 35 U.S.C. 112, second paragraph, is withdrawn in view of Applicant's amendment.

Claim Objections

4. Claims 1 and 18 are objected to because of the following informalities: The claims recite, "event selection control register (ECSR)." As indicated in claims 32 and 40, the acronym was likely intended to read --ESCR--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3, 4, 7-9, 18, 20, 21 and 27-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,835,705 to Larsen et al. (art of record, "Larsen") in view of U.S. Patent No. 6,205,468 to Diepstraten et al. (art of record, "Diepstraten") in view of U.S. Patent No. 5,657,253 to Dreyer et al. (art of record, "Dreyer").

With respect to claim 1 (currently amended), Larsen discloses an apparatus comprising:

(a) a processor to execute a plurality of threads simultaneously, each thread including a series of instructions and resulting in an event (see, for example, processor 10 in FIG. 1, and column 3, lines 39-55, which shows that the multithreaded processor simultaneously executes at least two threads, i.e. a plurality of threads, each comprising a group of instructions, and see, for example, column 6, lines 58-61, which shows that the threads result in events);

(b) an event selection control register (ECSR) (see, for example, control registers 80 in FIG. 2);

(c) a first multiplexer coupled to the ECSR to select a class of events, based on a first set of control signals from the ECSR, from a group of event signals issued from the processor (see, for example, multiplexer 82 in FIG. 2, and column 5, lines 9-17, which shows that the multiplexer selects events based on the control registers, and see, for example, blocks 176, 184 and 192 in FIG. 4, and column 5, lines 41-43, which shows selecting a group or class of events from the event signals of the processor).

Although Larsen discloses selecting an event that is not masked based on the control registers (see, for example, column 5, lines 9-17), Larsen does not expressly disclose:

(d) a second multiplexer coupled to the ECSR and the first multiplexer to mask, based on a second set of control signals from the ESCR, subclasses of the class of events in order to select an event that belongs to a subclass that is not masked.

However, Diepstraten discloses an event masker coupled to a control register for masking events based on control signals from the control register, to yield subclasses of the events that are not masked (see, for example, event mask register 90 in FIG. 3, and column 4, lines 42-50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the apparatus of Larsen with the event masking features of Diepstraten, such that the apparatus comprises a second multiplexer coupled to the ECSR and the first multiplexer to mask, based on a second set of control signals from the ESCR, subclasses of the class of events in order to select an event that belongs to a subclass that is not masked. One of

ordinary skill in the art would have been motivated to reduce the number of events that are to be processed (see, for example, Diepstraten, column 4, lines 42-50).

Although Diepstraten does not expressly disclose that the event masker is a multiplexer, Larson already suggests implementing such event selection as one or more multiplexers (see, for example, column 5, lines 30-36).

Larson in view of Diepstraten further discloses:

(e) a logic circuit coupled to the ESCR and the second multiplexer to qualify the event based on a thread ID, the thread ID indicating a source of the event including a thread of the plurality of threads where the event occurred (see, for example, Larsen, FIG. 3, and column 6, lines 10-23, which shows a logic circuit coupled to the multiplexer, and see, for example, Larsen, blocks 178 and 186 in FIG. 4, and column 6, line 54 to column 7, line 3, which shows qualifying the event based on the identity of the thread to which the event corresponds, i.e. the thread ID of the source thread of the plurality of threads where the event occurred, such as "thread 0" or "thread 1").

Although Larsen discloses qualifying the event based on a thread ID, Larsen does not expressly disclose qualifying the event based on a thread current privilege level (CPL).

However, Dreyer discloses a logic circuit coupled to an event selection control register and a multiplexer to qualify an event based on a thread current privilege level (CPL) (see, for example, logic block 23, control and event select register 17 and MUX 22 in FIG. 1, and column 4, lines 39-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the apparatus of Larsen and Diepstraten with the thread CPL features of

Dreyer, such that the apparatus comprises a logic circuit coupled to the ESCR and the second multiplexer to qualify the event based on a thread ID and a thread current privilege level (CPL). One of ordinary skill in the art would have been motivated to differentiate and qualify events based on supervisor and application levels of operation (see, for example, Dreyer, column 4, line 60 to column 5, line 3).

Larsen in view of Diepstraten in view of Dreyer further discloses:

(f) an event counter to count the event qualified by the logic circuit (see, for example, Larsen, performance monitor counters 84 in FIG. 2, and column 4, lines 50-57, which shows that the counters record or count the qualified events).

With respect to claim 3 (currently amended), the rejection of claim 1 is incorporated, and Larsen in view of Diepstraten in view of Dreyer further discloses the limitation wherein the ESCR comprises a first field of bits to store the first set of control signals to select the class of events (see, for example, Larsen, column 5, lines 9-17, which shows that the control registers have bit fields to store the control signals).

With respect to claim 4 (currently amended), the rejection of claim 3 is incorporated, and Larsen in view of Diepstraten in view of Dreyer further discloses the limitation wherein the ESCR further comprises a second field of bits to store the second set of control signals to mask the subclasses (see, for example, Diepstraten, event mask register 90 in FIG. 3, and see, for example, Larsen, column 5, lines 9-17, which shows that the control registers have bit fields to store the control signals).

With respect to claim 7 (previously presented), the rejection of claim 1 is incorporated, and Larsen in view of Diepstraten in view of Dreyer further discloses the limitation wherein the event counter is stopped and cleared before a new event is selected (see, for example, Larsen, column 4, lines 50-57, which shows software-writable event counters, and see, for example, Dreyer, column 3, lines 19-22, which shows resetting, i.e. stopping and clearing, the event counter with a software instruction).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Larsen with the counter reset features of Dreyer, so as to stop and clear the counter values in software.

With respect to claim 8 (previously presented), the rejection of claim 7 is incorporated, and Larsen in view of Diepstraten in view of Dreyer further discloses the limitation wherein the event counter is preset to a certain state (see, for example, Larsen, column 4, lines 50-57, which shows software-writable event counters, and see, for example, Dreyer, column 3, lines 19-22, which shows presetting the event counter to a certain value or state).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Larsen with the counter preset features of Dreyer, so as to enable functions such as countdowns (see, for example, Dreyer, column 4, lines 21-30).

With respect to claim 9 (previously presented), the rejection of claim 1 is incorporated, and Larsen in view of Diepstraten in view of Dreyer further discloses the limitation wherein the class of events includes hardware performance and breakpoint events (see, for example, Larsen, column 5, lines 47-56, which shows a class of events that includes hardware performance events

such as instructions completed and processor cycles, and breakpoint events such as thread switch counts).

With respect to claim 18 (currently amended), Larsen discloses a method comprising:

(a) executing a plurality of threads simultaneously, each thread including a series of instructions and resulting in an event (see, for example, processor 10 in FIG. 1, and column 3, lines 39-55, which shows that the multithreaded processor simultaneously executes at least two threads, i.e. a plurality of threads, each comprising a group of instructions, and see, for example, column 6, lines 58-61, which shows that the threads result in events);

(b) instructing a first multiplexer, based on a first set of signals from an event selection control register (ECSR), to select a class of events from a group of event signals issued from the processor (see, for example, control registers 80 and multiplexer 82 in FIG. 2, and column 5, lines 9-17, which shows instructing the multiplexer to select events based on the control registers, and see, for example, blocks 176, 184 and 192 in FIG. 4, and column 5, lines 41-43, which shows selecting a group or class of events from the event signals of the processor);

Although Larsen discloses selecting an event that is not masked based on the control registers (see, for example, column 5, lines 9-17), Larsen does not expressly disclose:

(c) instructing a second multiplexer, based on a second set of signals from the ECSR, to mask subclasses of the class of events in order to select an event that belongs to a subclass that is not masked.

However, Diepstraten discloses an event masker for masking events based on control signals from a control register, to yield subclasses of the events that are not masked (see, for example, event mask register 90 in FIG. 3, and column 4, lines 42-50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the method of Larsen with the event masking features of Diepstraten, such that the method comprises instructing a second multiplexer, based on a second set of signals from the ECSR, to mask subclasses of the class of events in order to select an event that belongs to a subclass that is not masked. One of ordinary skill in the art would have been motivated to reduce the number of events that are to be processed (see, for example, Diepstraten, column 4, lines 42-50).

Although Diepstraten does not expressly disclose that the event masker is a multiplexer, Larson already suggests implementing such event selection as one or more multiplexers (see, for example, column 5, lines 30-36).

Larson in view of Diepstraten further discloses:

(d) qualifying the event, by a logic circuit, based on a thread ID, the thread ID indicating a source of the event including a thread of the plurality of threads where the event occurred (see, for example, Larsen, FIG. 3, and column 6, lines 10-23, which shows a logic circuit, and see, for example, Larsen, blocks 178 and 186 in FIG. 4, and column 6, line 54 to column 7, line 3, which shows qualifying the event based on the identity of the thread to which the event corresponds, i.e. the thread ID of the source thread of the plurality of threads where the event occurred, such as "thread 0" or "thread 1").

Although Larsen discloses qualifying the event based on a thread ID, Larsen does not expressly disclose qualifying the event based on a thread CPL.

However, Dreyer discloses a logic circuit for qualifying an event based on a thread current privilege level (CPL) (see, for example, logic block 23, control and event select register 17 and MUX 22 in FIG. 1, and column 4, lines 39-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the method of Larsen and Diepstraten with the thread CPL features of Dreyer, such that the method comprises qualifying the event, by a logic circuit, based on a thread ID and a thread CPL. One of ordinary skill in the art would have been motivated to differentiate and qualify events based on supervisor and application levels of operation (see, for example, Dreyer, column 4, line 60 to column 5, line 3).

Larsen in view of Diepstraten in view of Dreyer further discloses:

(e) counting the event qualified by the logic circuit using an event counter (see, for example, Larsen, performance monitor counters 84 in FIG. 2, and column 4, lines 50-57, which shows that the counters record or count the qualified events); and

(f) accessing the event counter to determine a current count of the event (see, for example, Larsen, integer registers 38 in FIG. 1, and column 4, lines 57-61, which shows outputting the counter values to the integer registers, i.e. the access locations, and column 7, lines 40-52, which shows accessing the registers to determine a current count of the event).

With respect to claim 20 (previously presented), the rejection of claim 18 is incorporated, and Larsen in view of Diepstraten in view of Dreyer further discloses the limitation wherein the qualifying the event includes requiring that the event has a preselected thread ID (see, for example, Larsen, column 5, lines 27-30, which shows requiring that the event has a preselected thread ID such as "thread 0" or "thread 1").

With respect to claim 21 (previously presented), the rejection of claim 20 is incorporated, and Larsen in view of Diepstraten in view of Dreyer further discloses the limitation wherein the qualifying of the event further includes requiring that the event has a preselected thread CPL (see, for example, Dreyer, column 4, lines 49-58, which shows requiring that the event has a preselected thread CPL).

With respect to claim 27 (previously presented), the rejection of claim 18 is incorporated, and Larsen in view of Diepstraten in view of Dreyer further discloses the limitation wherein the thread CPL indicates a privilege level at which the thread at which the event occurred was operating when the event occurred (see, for example, Dreyer, column 4, lines 39-46, which shows that the CPL indicates a current privilege level at which the thread is operating when an event is to be counted).

With respect to claim 28 (previously presented), the rejection of claim 20 is incorporated, and Larsen in view of Diepstraten in view of Dreyer further discloses the limitation wherein the preselected thread ID represents a thread of the plurality of threads where the event occurred (see, for example, Larsen, column 6, line 54 to column 7, line 3, which shows that the thread ID represents the thread where the event occurred).

With respect to claim 29 (previously presented), the rejection of claim 21 is incorporated, and Larsen in view of Diepstraten in view of Dreyer further discloses the limitation wherein thread CPL indicates a privilege level at which the thread was operating at when the event

occurred (see, for example, Dreyer, column 4, lines 39-46, which shows that the CPL indicates a current privilege level at which the thread is operating when an event is to be counted).

With respect to claim 30 (previously presented), the rejection of claim 1 is incorporated, and Larsen in view of Diepstraten in view of Dreyer further discloses the limitation wherein the thread CPL indicates a privilege level at which the thread at which the event occurred was operating when the event occurred (see, for example, Dreyer, column 4, lines 39-46, which shows that the CPL indicates a current privilege level at which the thread is operating when an event is to be counted).

With respect to claim 31 (previously presented), the rejection of claim 1 is incorporated, and Larsen in view of Diepstraten in view of Dreyer further discloses an access location to allow access to the event counter to determine a current count of the event (see, for example, Larsen, integer registers 38 in FIG. 1, and column 4, lines 57-61, which shows outputting the counter values to the integer registers, i.e. the access locations, and column 7, lines 40-52, which shows accessing the registers to determine a current count of the event).

With respect to claim 32 (currently amended), Larsen discloses a system comprising:

(a) a storage medium coupled with a processor (see, for example, main memory 52 and processor 10 in FIG. 1), the processor to execute a plurality of threads simultaneously, each thread including a series of instructions and resulting in an event (see, for example, column 3, lines 39-55, which shows that the multithreaded processor simultaneously executes at least two threads, i.e. a plurality of threads, each comprising a group of instructions, and see, for example, column 6, lines 58-61, which shows that the threads result in events);

(b) an event selection control register (ESCR) coupled to the processor (see, for example, control registers 80 in FIG. 2);

(c) a first multiplexer coupled to the ESCR to select a class of events, based on a first set of control signals from the ESCR, from a group of event signals issued from the processor (see, for example, multiplexer 82 in FIG. 2, and column 5, lines 9-17, which shows that the multiplexer selects events based on the control registers, and see, for example, blocks 176, 184 and 192 in FIG. 4, and column 5, lines 41-43, which shows selecting a group or class of events from the event signals of the processor).

Although Larsen discloses selecting an event that is not masked based on the control registers (see, for example, column 5, lines 9-17), Larsen does not expressly disclose:

(d) a second multiplexer coupled to the ESCR and the first multiplexer to mask, based on a second set of control signals from the ESCR, subclasses of the class of events in order to select an event that belongs to a subclass that is not masked.

However, Diepstraten discloses an event masker coupled to a control register for masking events based on control signals from the control register, to yield subclasses of the events that are not masked (see, for example, event mask register 90 in FIG. 3, and column 4, lines 42-50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Larsen with the event masking features of Diepstraten, such that the system comprises a second multiplexer coupled to the ESCR and the first multiplexer to mask, based on a second set of control signals from the ESCR, subclasses of the class of events in order to select an event that belongs to a subclass that is not masked. One of

ordinary skill in the art would have been motivated to reduce the number of events that are to be processed (see, for example, Diepstraten, column 4, lines 42-50).

Although Diepstraten does not expressly disclose that the event masker is a multiplexer, Larson already suggests implementing such event selection as one or more multiplexers (see, for example, column 5, lines 30-36).

Larson in view of Diepstraten further discloses:

(e) a logic circuit coupled to the ESCR and the second multiplexer to qualify the event that is to be selected based on a thread ID, the thread ID indicating a source of the event including a thread of the plurality of threads where the event occurred (see, for example, Larsen, FIG. 3, and column 6, lines 10-23, which shows a logic circuit coupled to the multiplexer, and see, for example, Larsen, blocks 178 and 186 in FIG. 4, and column 6, line 54 to column 7, line 3, which shows qualifying the event based on the identity of the thread to which the event corresponds, i.e. the thread ID of the source thread of the plurality of threads where the event occurred, such as "thread 0" or "thread 1").

Although Larsen discloses qualifying the event based on a thread ID, Larsen does not expressly disclose qualifying the event based on a thread current privilege level (CPL).

However, Dreyer discloses a logic circuit coupled to an event selection control register and a multiplexer to qualify an event based on a thread current privilege level (CPL) (see, for example, logic block 23, control and event select register 17 and MUX 22 in FIG. 1, and column 4, lines 39-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Larsen and Diepstraten with the thread CPL features of

Dreyer, such that the system comprises a logic circuit coupled to the ESCR and the second multiplexer to qualify the event that is to be selected based on a thread ID and a thread current privilege level (CPL). One of ordinary skill in the art would have been motivated to differentiate and qualify events based on supervisor and application levels of operation (see, for example, Dreyer, column 4, line 60 to column 5, line 3).

Larsen in view of Diepstraten in view of Dreyer further discloses:

(f) an event counter to count the event qualified by the logic circuit (see, for example, Larsen, performance monitor counters 84 in FIG. 2, and column 4, lines 50-57, which shows that the counters record or count the qualified events); and

(g) an access location to allow access to the event counter to determine a current count of the event (see, for example, Larsen, integer registers 38 in FIG. 1, and column 4, lines 57-61, which shows outputting the counter values to the integer registers, i.e. the access locations, and column 7, lines 40-52, which shows accessing the registers to determine a current count of the event).

With respect to claim 33 (previously presented), the rejection of claim 32 is incorporated, and Larsen in view of Diepstraten in view of Dreyer further discloses the limitation wherein the access location allows access to determine the count without disturbing the operation of event counter (see, for example, Larsen, column 7, lines 40-52, which shows accessing the registers to read the count without disturbing the operation of the counters).

With respect to claim 34 (currently amended), the rejection of claim 33 is incorporated, and the limitations recited in the claim are analogous to those of claim 3 (see the rejection of claim 3 above).

With respect to claim 35 (currently amended), the rejection of claim 34 is incorporated, and the limitations recited in the claim are analogous to those of claim 4 (see the rejection of claim 4 above).

With respect to claim 36 (previously presented), the rejection of claim 32 is incorporated, and the limitations recited in the claim are analogous to those of claim 7 (see the rejection of claim 7 above).

With respect to claim 37 (previously presented), the rejection of claim 36 is incorporated, and the limitations recited in the claim are analogous to those of claim 8 (see the rejection of claim 8 above).

With respect to claim 38 (currently amended), the rejection of claim 32 is incorporated, and the limitations recited in the claim are analogous to those of claim 9 (see the rejection of claim 9 above).

With respect to claim 39 (previously presented), the rejection of claim 32 is incorporated, and the limitations recited in the claim are analogous to those of claim 30 (see the rejection of claim 30 above).

With respect to claim 40 (currently amended), Larsen discloses a machine-readable medium having stored thereon data representing sets of instructions (see, for example, column 3, lines 11-19, which shows a machine-readable medium having instructions stored thereon), the sets of instructions which, when executed by a machine (see, for example, column 4, lines 25-28, which shows executing the instructions), cause the machine to:

(a) execute a plurality of threads simultaneously, each thread including a series of instructions and resulting in an event (see, for example, processor 10 in FIG. 1, and column 3, lines 39-55, which shows that the multithreaded processor simultaneously executes at least two threads, i.e. a plurality of threads, each comprising a group of instructions, and see, for example, column 6, lines 58-61, which shows that the threads result in events);

(b) instruct a first multiplexer, based on a first set of signals from an event selection control register (ESCR), to select a class of events from a group of event signals issued from the processor (see, for example, control registers 80 and multiplexer 82 in FIG. 2, and column 5, lines 9-17, which shows instructing the multiplexer to select events based on the control registers, and see, for example, blocks 176, 184 and 192 in FIG. 4, and column 5, lines 41-43, which shows selecting a group or class of events from the event signals of the processor);

Although Larsen discloses selecting an event that is not masked based on the control registers (see, for example, column 5, lines 9-17), Larsen does not expressly disclose:

(c) instruct a second multiplexer, based on a second set of signals from the ESCR, to mask subclasses of the class of events in order to select an event that belongs to a subclass that is not masked.

However, Diepstraten discloses an event masker for masking events based on control signals from a control register, to yield subclasses of the events that are not masked (see, for example, event mask register 90 in FIG. 3, and column 4, lines 42-50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the machine-readable medium of Larsen with the event masking features of Diepstraten, such that the machine is caused to instruct a second multiplexer, based on a second set of control signals from the ESCR, to mask subclasses of the class of events in order to select an event that belongs to a subclass that is not masked. One of ordinary skill in the art would have been motivated to reduce the number of events that are to be processed (see, for example, Diepstraten, column 4, lines 42-50).

Although Diepstraten does not expressly disclose that the event masker is a multiplexer, Larson already suggests implementing such event selection as one or more multiplexers (see, for example, column 5, lines 30-36).

Larson in view of Diepstraten further discloses:

(d) qualify the event, by a logic circuit, based on a thread ID, the thread ID indicating a source of the event including a thread of the plurality of threads where the event occurred (see, for example, Larsen, FIG. 3, and column 6, lines 10-23, which shows a logic circuit, and see, for example, Larsen, blocks 178 and 186 in FIG. 4, and column 6, line 54 to column 7, line 3, which shows qualifying the event based on the identity of the thread to which the event corresponds, i.e. the thread ID of the source thread of the plurality of threads where the event occurred, such as "thread 0" or "thread 1").

Although Larsen discloses qualifying the event based on a thread ID, Larsen does not expressly disclose qualifying the event based on a thread CPL.

However, Dreyer discloses a logic circuit for qualifying an event based on a thread current privilege level (CPL) (see, for example, logic block 23, control and event select register 17 and MUX 22 in FIG. 1, and column 4, lines 39-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the machine-readable medium of Larsen and Diepstraten with the thread CPL features of Dreyer, such that the machine is caused to qualify the event, by a logic circuit, based on a thread ID and a thread CPL. One of ordinary skill in the art would have been motivated to differentiate and qualify events based on supervisor and application levels of operation (see, for example, Dreyer, column 4, line 60 to column 5, line 3).

Larsen in view of Diepstraten in view of Dreyer further discloses:

(e) count the event qualified by the logic circuit using an event counter (see, for example, Larsen, performance monitor counters 84 in FIG. 2, and column 4, lines 50-57, which shows that the counters record or count the qualified events); and

(f) access the event counter to determine a current count of the event (see, for example, Larsen, integer registers 38 in FIG. 1, and column 4, lines 57-61, which shows outputting the counter values to the integer registers, i.e. the access locations, and column 7, lines 40-52, which shows accessing the registers to determine a current count of the event).

With respect to claim 41 (currently amended), the rejection of claim 40 is incorporated, and the limitations recited in the claim are analogous to those of claim 20 (see the rejection of claim 20 above).

With respect to claim 42 (currently amended), the rejection of claim 41 is incorporated, and the limitations recited in the claim are analogous to those of claim 21 (see the rejection of claim 21 above).

With respect to claim 43 (previously presented), the rejection of claim 40 is incorporated, and the limitations recited in the claim are analogous to those of claim 27 (see the rejection of claim 27 above).

With respect to claim 44 (previously presented), the rejection of claim 40 is incorporated, and the limitations recited in the claim are analogous to those of claim 28 (see the rejection of claim 28 above).

With respect to claim 45 (previously presented), the rejection of claim 41 is incorporated, and the limitations recited in the claim are analogous to those of claim 29 (see the rejection of claim 29 above).

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (571) 272-3707. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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